METHODOLOGY FOR FIXING Qcrit AT DESIGN TIMING IMPACT

Abstract

A method and system for simulating an integrated circuit. The method includes the steps of performing a timing analysis of the circuits to ensure that they meet specified timing criteria, performing soft error analysis of the circuits to determine whether they meet specified soft error criteria, and improving those circuits that fail the soft error analysis to improve their resistance to soft errors and having no degradation on timing. Preferably, the improving step includes the step of improving those circuits that fail the soft error analysis by either having an additional voltage source or altering the capacitance of the circuits.